Three-Dimensional MMIC Technology: A Possible Solution to Masterslice MMIC's on GaAs and Si

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***Abstract*—A novel masterslice MMIC is presented that expands the possibilities for three-dimensional (or multilayer) MMIC technology. This MMIC incorporates two levels of ground metals, resulting in an effective selection of master-array elements on the wafer surface by using the lower-level metal and a circuit-stacking effect by the upper one. X-band amplifier and receiver MMIC's on 3 × 1 and 6 × 3 array-units, respectively, are also demonstrated in very small areas.**

I. Introduction

MANY single-chip receiver MMIC's have been recently fabricated in planar forms [1] to cover IMS, DBS, and higher-frequency bands reaching into the V-band. However, integration level I, defined as gain (G in dB)-bandwidth ($\Delta f/f_0$) product per mm^2, decreases along a curve of $I \times [f(\mathrm{GHz})]^{1/2} = 2$ ($I < 0.9$ above 5 GHz). Employing 3-D (or multilayer) MMIC's, which use thin polyimide-film layers on GaAs wafers, is an effective method for significantly increasing I [2]–[7]. The largest I reaches to 2 in the X-band [6], that is to say a threefold increase in comparison to that of planar ones. The reasons for this are that passive circuits are designed with a narrow line-width and a spacing of less than 30 μm due to the polyimide layers, which are as thin as 2.5 μm each, and that these circuits are stacked up in the upper and lower levels of the polyimide layers [3], [5]. However, in both types of MMIC's, planar and 3-D, each new development requires its own mask set and fabrication process for semiconductor device arrangement and passive circuit layout, resulting in a high development cost.

In this letter, we present a novel masterslice-MMIC structure that expands the advantages of the 3-D MMIC. The structure effectively uses a ground metal that partially covers the master-array units on the surface of a wafer, creating a space wide enough for the 3-D circuits stacked above it. Amplifier and receiver MMIC's on 3 × 1 and 6 ×3 master-array units, respectively, will also be described.

II. Structure

The most significant feature of the masterslice MMIC structure is that two levels of ground metals are incorporated into the 3-D structure. Fig. 1(a) shows the basic structure of the masterslice MMIC. Many units, each of which contains transistors, resistors, and lower electrodes for MIM capacitors, are located repeatedly (nearly 6 units/mm^2) on a GaAs or Si wafer to form a master array, and the entire wafer surface is passivated. The on-wafer elements, which are not selected for microwave circuit design, are covered with a ground metal, GND1. Both thin polyimide layers and an additional ground metal, GND2, are stacked over the wafer and GND1 to complete the 3-D MMIC design. Therefore, a space for many miniature passive circuits is created over GND1, where the upper electrodes of MIM capacitors are used for GND1 in order to maximize the space. GND1 and the polyimide film layers provide passive circuits that are independent of the substrate properties: semi-insulating or conductive.

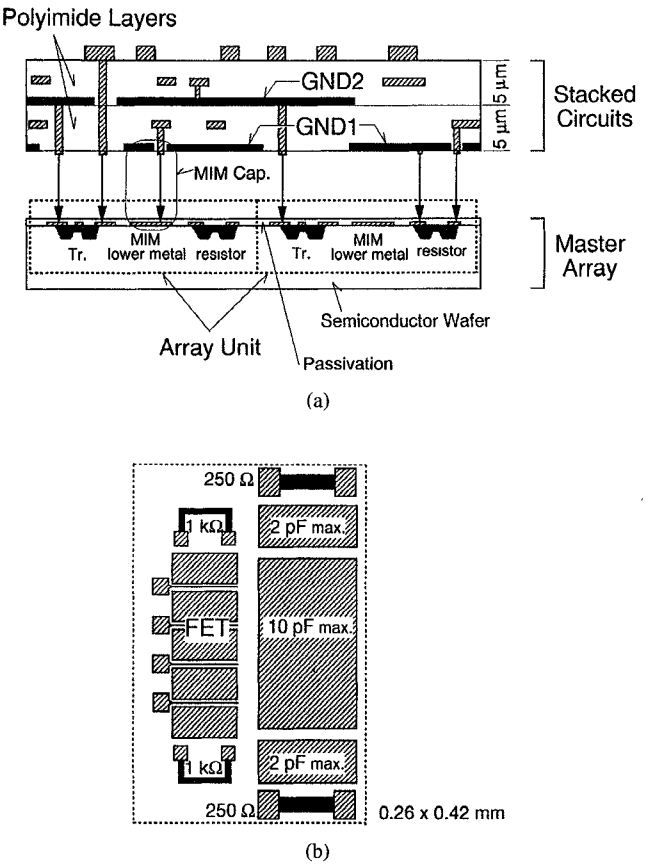

Fig. 1. Masterslice MMIC structure and an array-unit configuration. (a) Basic structure for the masterslice MMIC. (b) Array unit.

An array unit used for the following applications is illustrated in Fig. 1(b). The array unit (0.26 × 0.42 mm) is designed to contain a 200-μm gate-width FET, resistors, and

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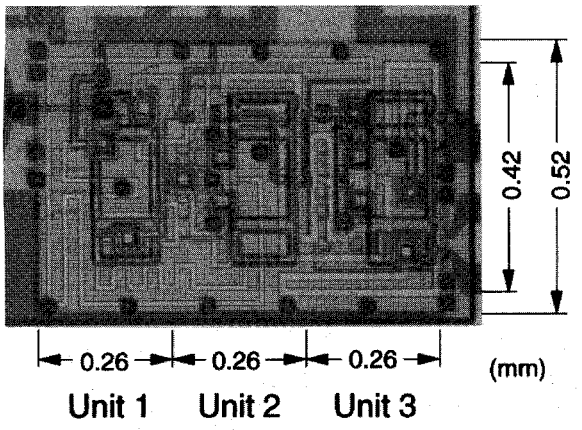

Fig. 2. Photomicrograph of a 9–12.5-GHz masterslice-MMIC amplifier.

two types of lower conductors for MIM capacitors, from which the maximum capacitances are 2 and 10 pF, respectively.

III. Circuit Design

A. Amplifier

A photomicrograph of a 9–12.5-GHz, 8-dB gain masterslice-MMIC amplifier measuring 0.78 × 0.52 mm is shown in Fig. 2, where three array units arranged side-by-side are used. This single-stage amplifier employs a cascode FET that connects a common-source-FET in unit 2 and a common-gate-FET in unit 3 with a nearly 2-mm-length thin-film microstrip (TFMS) line [2], [3] to achieve a higher matching gain and wider frequency range. GND2 and each strip metal above it, in Fig. 1(a), forms the TFMS line. The three 10-pF capacitors in the units are used for RF short, two and one 2-pF max. capacitors in unit 1 and unit 3, respectively, are either in series or shunt, and the 250-Ω resistor in unit 1 and 1-kΩ resistor in unit 3 are for dc bias. Capacitances for the series and shunt capacitors were determined by the MIM upper electrode areas. The other array-elements and the MIM lower electrode areas, except for that of the series capacitors, are covered using GND1. The TFMS lines for impedance matching are located above GND2. The thin-film strip lines between GND1 and GND2 are used for dc-bias feed, access to resistors, and connecting FET electrodes. The capacitive coupling effect between the FET electrodes and GND2 above the FET was considered in the amplifier design. The frequency characteristics of the amplifier are shown in Fig. 3. The noise figure is nearly 5.5 dB and a 30-dB gain control is provided by the second-FET gate voltage.

B. Single-Chip Receiver

X-band, single-chip receiver MMIC's were designed for the pattern-layout feasibility in a 2 × 2 mm GaAs die, using the masterslice-MMIC design rule. Fig. 4 shows an example of the single-chip MMIC's, where 6 × 3 units are arrayed in an area of 1.8 × 1.8 mm. A three-stage variable-gain amplifier is located on the left half, an image-rejection mixer composed of a pair of single mixers and a Wilkinson divider and a

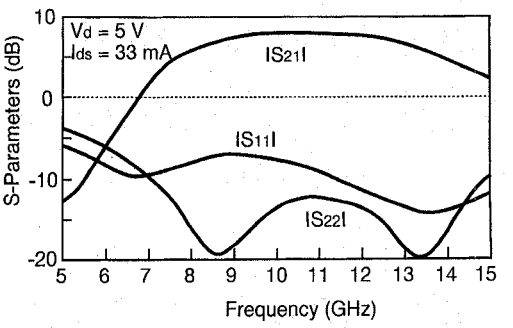

Fig. 3. Frequency characteristics of the masterslice-MMIC amplifier.

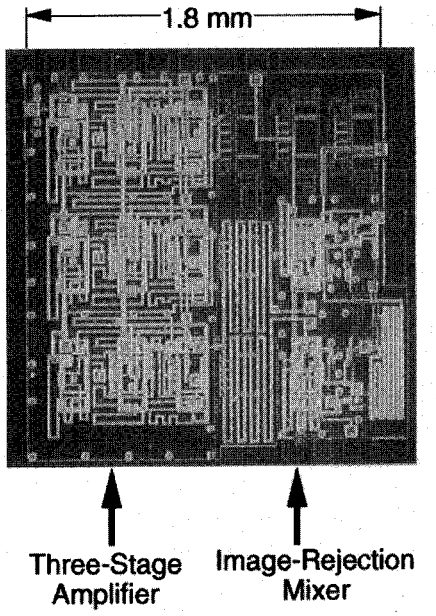

Fig. 4. Photomicrograph of a single-chip receiver MMIC fabricated on 6 × 3 array-units.

90° broadside coupler [7] is located on the lower side of the right half, and room is left unused in the upper portion of the right half. A portion of the array shows through the unused area in GND2. In the three-stage amplifier, amplifiers are directly cascode-connected by reconfiguring the output and input matching-circuit layout. The GND2 metal under the divider and coupler, which use high-impedance lines, is removed so as to provide them with the full thickness of the polyimide layers (10 μm). As shown in Fig. 4, the 3-D masterslice-MMIC technology is much more suitable for single-chip integration on a single footprint, therefore it is an effective way to quickly response to the MMIC market.

IV. Conclusion

A 3-D masterslice MMIC technology has been demonstrated through our experimental study. This MMIC will prove itself cost-effective in production and responsive to a rapidly changing MMIC market. Another feature of this technology is that it can be used for both GaAs and Si MMIC's due to the effect of GND1. Applying this technology to Si MMIC is expected to significantly extend the maximum operating frequency of Si MMIC.

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